[0024] The semiconductor device **1** illustrated in FIG. **1** and FIG. **2** is a power semiconductor device (e.g., an IEGT (Injection Enhanced Gate Transistor)) and includes a collector electrode **80** which is a first main electrode, a p-type collector layer **11**, an n^--type base layer **13**, an n-type barrier layer **14**, a p-type diffusion layer **15**, a p-type base layer **16**, an n^+-type emitter layer **17**, trenches **20**, **23**, and **26**, and the emitter electrode **81** which is a second main electrode. Herein, "collectors" may be referred to as "drains;" and "emitters" may be referred to as "sources." The n-type impurity conductivity type is taken as a first conductivity type; and the p-type is taken as a second conductivity type.

[0025] In the semiconductor device **1** as illustrated in FIG. **1**, the p-type collector layer **11** is provided on the collector electrode **80** (the first main electrode). An n-type buffer layer **12** is provided on the p-type collector layer **11**. The n^--type base layer **13** is provided on the n-type buffer layer **12**. The impurity concentration of the n^--type base layer **13** is lower than the impurity concentration of the n-type buffer layer **12**. The n^--type base layer **13** functions as a drift layer.

[0026] The n-type barrier layer **14** and the p-type diffusion layer **15** are provided on the n^--type base layer **13**. The n-type barrier layer **14** and the p-type diffusion layer **15** are alternately arranged on the n^--type base layer **13**. The impurity concentration of the n-type barrier layer **14** is higher than the impurity concentration of the n^--type base layer **13**. The upper face of the n-type barrier layer **14** is lower than the upper face of the p-type diffusion layer **15**. Restated, the n-type barrier layer **14** is formed with a protruding configuration from the major surface of the n^--type base layer **13** toward the p-type diffusion layer **15** side. The p-type base layer **16** is provided on the n-type barrier layer **14**. The n^+-type emitter layer **17** and a p^+-type contact layer **18** are provided selectively in the surface of the p-type base layer **16**. Multiple trenches are made with trench configurations from the surfaces of the p-type base layer **16** and the p-type diffusion layer **15** toward the collector electrode **80** side. The trenches are provided between the p-type base layer **16** and the p-type diffusion layer **15** and between the n-type barrier layer **14** and the p-type diffusion layer **15**.

[0027] For example, the n-type barrier layer **14** is interposed in the p-type diffusion layer **15**. Thereby, two pn junction interfaces exist on two sides of the n-type barrier layer **14**. One of the two pn junction interfaces is indicated by arrow A in the drawings; and the pn junction interface on the side opposite to arrow A is indicated by arrow B.

[0028] The trench **20** is made with a trench configuration from the surfaces of the p-type base layer **16** and the n^+-type emitter layer **17** toward the collector electrode **80** side at the junction interface between the n-type barrier layer **14** and the p-type diffusion layer **15** indicated by arrow A. A conductor layer **22** made of, for example, polysilicon is provided inside the trench **20** with an insulating film **21** such as an oxide film interposed. The bottom faces (the lower faces) of the p-type diffusion layer **15** and the n-type barrier layer **14** are positioned on the collector electrode **80** side of the lower end of the trench **20**. The n-type barrier layer **14** and the p-type diffusion layer **15** form a super junction proximally to the tip (proximally to the lower end) of the trench **20**.

[0029] The trench **23** is made with a trench configuration from the surfaces of the p-type base layer **16** and the n^+-type emitter layer **17** toward the collector electrode **80** side at the junction interface between the n-type barrier layer **14** and the p-type diffusion layer **15** indicated by arrow B. A conductor layer **25** made of, for example, polysilicon is provided inside the trench **23** with an insulating film **24** such as an oxide film interposed. The bottom faces of the p-type diffusion layer **15** and the n-type barrier layer **14** are positioned on the collector electrode **80** side of the lower end of the trench **23**. The n-type barrier layer **14** and the p-type diffusion layer **15** form a super junction proximally to the tip of the trench **23**.

[0030] In the semiconductor device **1**, the trench **26** is provided with a trench configuration between the trench **20** and the trench **23**. The trench **26** pierces the n^+-type emitter layer **17** and the p-type base layer **16** to reach the n-type barrier layer **14**. A conductor layer **28** made of, for example, polysilicon is provided inside the trench **26** with an insulating film **27** such as an oxide film interposed. The trench **20**, the trench **23**, and the trench **26** have substantially the same depth.

[0031] Thus, in the semiconductor device **1**, the bottom faces of the p-type diffusion layer **15** and the n-type barrier layer **14** are positioned on the collector electrode **80** side of the lower ends of the trenches **20**, **23**, and **26**. The conductor layer **28** is a trench gate electrode (a control electrode) of the semiconductor device **1** and is electrically connected to a gate interconnect (not illustrated). The conductor layer **28** is a control electrode configured to control the current flow between the n^+-type emitter layer **17** and the n-type barrier layer **14**.

[0032] The p^+-type contact layer **18** and the n^+-type emitter layer **17** are electrically connected to the emitter electrode **81** (the second main electrode). The conductor layer **22** inside the trench **20** and the conductor layer **25** inside the trench **23** are electrically connected to the emitter electrode **81**. Thereby, the potential of the conductor layer **28** which is the trench gate electrode is shielded by the conductor layer **22** and the conductor layer **25** provided on the two sides of the conductor layer **28**. In other words, the conductor layer **22** and the conductor layer **25** function as electrical shield layers of the conductor layer **28**. The insulating layer **70** is provided on the surfaces of the p-type diffusion layer **15**, the p-type base layer **16**, the n^+-type emitter layer **17**, and the trenches **20**, **23**, and **26**.

[0033] In the semiconductor device **1** as illustrated in FIG. **2**, each of the trenches **20**, **23**, and **26** extend in substantially parallel stripe configurations. The extension direction is, for example, a direction substantially parallel to the major surface of the n^--type base layer **13**. The p^+-type contact layer **18** is provided adjacent to the n^+-type emitter layer **17**.

[0034] Referring to FIG. **1** and FIG. **2**, the n^+-type emitter layer **17** is positioned on two sides of the trench **26** and contacts the side faces of the trench **26**. The p-type base layer **16** contacts the side face of the trench **20** or the side face of the trench **23**. The p-type base layer **16** is provided under the n^+-type emitter layer **17** and the p^+-type contact layer **18**. The p-type base layer **16** is electrically connected to the emitter electrode **81** via the n^+-type emitter layer **17** or the p^+-type contact layer **18**.

[0035] The width of the n-type barrier layer **14** interposed in the p-type diffusion layer **15** is narrower than the width of the p-type diffusion layer **15**, where the "width" of the members in the semiconductor device **1** is defined as the width in a direction which is substantially perpendicular to the direction in which the trenches **20**, **23**, and **26** extend in stripe configurations and is substantially parallel to the major surface of the n^--type base layer **13**.

[0036] For example, the width of a main cell **90** is narrower than the width of a sub-cell **91**, where the main cell **90** is taken